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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Term: (buffer near2 fullness near2 control$4)

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Terms	Documents
L7 and ((375/$3)!.CCLS.)	420

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L8

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Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L8	L7 and ((375/$3)!.CCLS.)	420	L8
L7	(receiver near3 buffer near$ fullness near3 control$3) same (modem$)	2053	L7
L6	(receiver near3 buffer near$2 full$3 near3 control$3) same (modem$)	2046	L6
L5	(receiver near3 buffer near$2 (full$3 or overun$) near3 control$3) same (modem$)	2046	L5
L4	(receiver near3 buffer near$2 control$3) same (full$3) same (delet or compres$4) same (modem$)	123	L4
L3	(receiver near3 buffer near$2 control$3) same full$3 same (delet or compres$4) same (modem$)	123	L3
L2	(buffer near$2 control$3) same full$3 same (delet or compres$4) same (modem$)	135	L2
L1	(buffer near$2 control$3) same full$3 same (delet or compres$4)same (modem$)	135	L1

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L13: Entry 2 of 2 File: USPT Jun 16, 1992

DOCUMENT-IDENTIFIER: US 5122875 A
TITLE: An HDTV compression system

Abstract Text (1):
Apparatus for encoding/decoding a HDTV signal for e.g., terrestrial transmission includes a compression circuit responsive to high definition video source signals for providing ierarchically layered codewords CW representing compressed video data and associated codewords T, defining the types of data represented by the codewords CW. A priority selection circuit, responsive to the codewords CW and T, parses the codewords CW into high and low priority codeword sequences wherein the high and low priority codeword sequences correspond to compressed video data of relatively greater and lesser importance to image reproduction respectively. A transport processor, responsive to the high and low priority codeword sequences, forms high and low priority transport blocks of high and low priority codewords respectively. Each transport block includes a header, codewords CW and error detection check bits. The respective transport blocks are applied to an forward error check circuit for applying additional error check data. Thereafter the high and low priority data are applied to a modem wherein they quadrature amplitude modulate respective carriers for transmission.

Brief Summary Text (13):
The present invention includes apparatus for encoding/decoding a HDTV signal for, w.g., terrestrial transmission. A first embodiment corresponding to a HDTV signal encoder includes a compression circuit responsive to high definition video source signals for providing hierarchically layered codewords CW representing compressed video data and associated codewords T, defining the types of data represented by the codewords CW. A priority selection circuit, responsive to the codewords CW and T, parses the codewords CW into high and low priority codeword sequences wherein the high and low priority codeword sequences correspond to compressed video data of relatively greater and lesser importance to image reproduction respectively. A transport processor, responsive to the high and low priority codeword sequences, forms high and low priority transport blocks of high and low priority codewords respectively. Each transport block includes a header, codewords CW and error detection check bits. The respective transport blocks are applied to an forward error check circuit for applying additional error check data. Thereafter the high and and low priority data are applied to a modem wherein they quadrature amplitude modulate respective carriers for transmission.

Brief Summary Text (14):
A further embodiment, corresponding to a HDTV signal decoder, includes a modem responsive to transmitted signal for recovering the high and low priority signals from the transmitted signal. The high and low priority signals are coupled to an error correction circuit, which, responsive to said additional error check data performs, e.g., Reed-Solomon error correction on the received data. High and low priority data provided from the error correction circuit are applied to a transport processor. The transport processor excises transport block header information and error detection check bits from the data stream and provides respective sequences of high and low priority codewords, and transport header information. A priority deselect circuit, responsive to the sequences of high and low priority codewords and the transport header information combines the sequences of high and low priority codewords into a sequence of hierarchically layered codewords CW representing compressed video data. This sequence is coupled to a decompression circuit for generating a decompressed video signal representing HDTV images.

Drawing Description Text (15):

FIG. 11 is a block diagram of exemplary circuitry which may be implemented for the MODEMS 17 and 20 of FIG. 1.

Detailed Description Text (16):
The HP and LP data streams from the transport processor 12 are applied to the respective rate buffers 13 and 14, which convert the variable rate compressed video data from the processor 12 to data occurring at a substantially constant rate. The rate adjusted HP and LP data are coupled to forward error encoding elements 15 and 16 which a) perform REED SOLOMON forward error correction encoding independently to the respective data streams; b) interleave blocks of data to preclude large error bursts from corrupting a large contiguous area of a reproduced image; and c) appends, e.g., Barker codes to the data for synchronizing the data stream at the receiver. Thereafter the signals are coupled to a transmission modem wherein the HP channel data quadrature amplitude modulates a first carrier and the LP channel data quadrature amplitude modulates a second carrier displaced from the first carrier by approximately 2.88 MHz. The 6 dB bandwidth of the modulated first and second carriers are respectively about 0.96 MHz and 3.84 MHz. The modulated first carrier is transmitted with approximately 9 dB greater power than the modulated second carrier. Since the HP information is transmitted with greater power it is much less prone to corruption by the transmission channel. The HP carrier is located in the portion of the frequency spectrum of an, e.g., NTSC TV, transmission channel normally occupied by the vestigial sideband of a standard NTSC TV signal. This portion of the signal channel is normally significantly attenuated by the Nyquist filters of standard receivers and thus HDTV signals with this transmission format will not introduce cochannel interference.

Detailed Description Text (17):
At the receiver the transmitted signal is detected by the modem 20 which provides two signals corresponding to the HP and LP channels. These two signals are applied to respective REED SOLOMON error correcting decoders 21 and 22. The error corrected signals are coupled to rate buffers 23 and 24 which receive data at a variable rate commensurate with the requirements of the subsequent decompression circuitry. The variable rate HP and LP data is applied to a transport processor 25 which performs the inverse process of the processor 12. In addition it performs a degree of error detection responsive to the parity check bits included in the respective transport blocks. The transport processor 25 provides separated auxiliary data, HP data, LP data and an error signal E. The latter three signals are coupled to a priority deselect processor 26 which reformats the HP and LP data into an hierarchically layered signal which is applied to a decompressor 27. The decompressor 27 performs the inverse function of the compressor 27.

Detailed Description Text (78):
FIG. 11 illustrates exemplary modem circuitry for both the transmitting and receiving ends of the system. HP and LP data from the forward error correction circuits 15 and 16 are applied to respective 64 QAM modulators 400 and 401. The modulator 400 provides an HP analog signal with a -6 dB bandwidth of approximately 0.96 MHZ. This signal is applied to a 1.5 MHZ band pass filter 402 to eliminate high frequency harmonics, and then is applied to an analog signal summer 405. The modulator 401 provides an LP analog signal with a -6 dB bandwidth of approximately 3.84 MHZ. This signal is applied to a 6 MHZ band pass filter 404 to eliminate high frequency harmonics, and then is applied to an attenuator 406. The attenuator 406 reduces the amplitude of the LP analog signal by approximately 9 dB relative to the HP analog signal. The attenuated LP signal is then coupled to the analog signal summer 405, wherein it is summed with the analog HP signal to produce a signal with a frequency spectrum similar to the signal spectrum shown in FIG. 1. The combined signal is applied to a mixer 407 wherein it is multiplied by an RF carrier to frequency translate the combined signal to a frequency band that comports with a standard TV transmission channel. The translated signal is then applied to a band pass filter 408, which tailors the spectral characteristics of the frequency translated signal to fit within the standard channel.

CLAIMS:

4. The apparatus set forth in claim 2 wherein said first means includes means, responsive to a control signal for adaptively controlling the volume of said

compressed version of said video signals; and

wherein said rate buffers include means for providing a signal indicating the relative fullness of said rate buffers; and

means responsive to said signal indicating the relative fullness of said rate buffers for generating said control signal.

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L12: Entry 2 of 78 File: USPT Dec 11, 2001

DOCUMENT-IDENTIFIER: US 6330286 B1
TITLE: Flow control, latency control, and bitrate conversions in a timing correction and frame synchronization apparatus

Detailed Description Text (33):
The method for using the delay time S304 to control the fullness of the decoder buffer is as follows. The adjusted PCRB is used as the DTS entry. When a video PES is present at the output of the video buffer at the decoder, the DTS (Decode Time Stamp) contained in the PES header is compared to the PCRB real-time clock reference derived from the PCR (Program Clock Reference) packets in the transport stream. The PES must await alignment of the DTS with the recovered PCRB. This alignment takes place after the period of time that the value of the delay time S304 indicates, because the delay time S304 was added to the PCRB at the encoder, and this adjusted PCRB is used as the DTS entry.

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L12: Entry 27 of 78 File: USPT Jan 20, 1998

DOCUMENT-IDENTIFIER: US 5710595 A
TITLE: Method and apparatus for controlling quantization and buffering for digital signal compression

Brief Summary Text (14):
The present invention provides an improved method of buffering and controlling the encoder buffer fullness by limiting the Q-step value to a predetermined maximum. This maximum or threshold is set to a value that provides a tolerable level of image quality degradation. According to one aspect of the present invention, when the buffer fullness would ordinarily require an excessively high Q-step value for a subsequent frame, the present invention makes other adjustments, such as skipping the next frame to be encoded or increasing the target buffer fullness. As a result, adjustment of the Q-step value may be limited, thus improving video frame display quality.

Detailed Description Text (7):
The processor 30 further determines whether too many consecutive frames are scheduled to be skipped. If so, then the processor 30 increases the target fullness of the encoder buffer 26. Increasing the target buffer fullness, however, may increase the delay in frame transmission. Nevertheless, the delay added by increasing the buffer fullness may sometimes be less detrimental than skipping another frame. Such control of the target buffer fullness, as well as the number of frames to be skipped, is discussed in further detail below in connection with FIG. 2.

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L14	l12 and $dsl	0	L14
L13	L12 and modem$	2	L13
L12	(buffer near2 fullness near2 control$4)	78	L12
L11	(buffer near2 fullness near2 control$4) same (modem$)	0	L11
L10	(buffer near2 fullness near2 control$4 near2 (delet or compres$4)) same (modem$)	0	L10
L9	(buffer near fullness near control$3 near2 (delet or compres$4)) same (modem$)	0	L9
L8	L7 and ((375/$3)!.CCLS.)	420	L8
L7	(receiver near3 buffer near$ fullness near3 control$3) same (modem$)	2053	L7
L6	(receiver near3 buffer near$2 full$3 near3 control$3) same (modem$)	2046	L6
L5	(receiver near3 buffer near$2 (full$3 or overun$) near3 control$3) same (modem$)	2046	L5
L4	(receiver near3 buffer near$2 control$3) same (full$3) same (delet or compres$4) same (modem$)	123	L4
L3	(receiver near3 buffer near$2 control$3) same full$3 same (delet or compres$4) same (modem$)	123	L3
L2	(buffer near$2 control$3) same full$3 same (delet or compres$4) same (modem$)	135	L2
L1	(buffer near$2 control$3) same full$3 same (delet or compres$4)same (modem$)	135	L1

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L12: Entry 13 of 78 File: USPT Sep 7, 1999

DOCUMENT-IDENTIFIER: US 5949488 A
TITLE: Video signal encoding system controller

Detailed Description Text (4):
On the other hand, the controller 10 receives the differential and the current frame data provided from the DPCM block 20 and a signal notifying fullness of the buffer 60 provided therefrom. The controller 10 of the present invention serves to determine the inter/intra mode, the field/frame DCT mode and the quantization parameter on a macroblock basis and provide signals to notify the former two to the DPCM block 20 and the last one to the Q block 30. In response to the inter/intra mode signal, the DPCM block 20 provides the differential frame data and the current frame data (inter mode), or the current frame data itself (intra mode) to the DCT block 25. The difference or the current frame data is provided in a unit of an 8.times.8 block and 8.times.8 DCT is performed therefor. Format of such blocks provided from the DPCM block 20 to the DCT block 25 depends on the field/frame DCT mode signal. In case of the frame DCT mode, the DPCM block 20 provides frame-organized blocks while in case of the field DCT mode, it provides field-organized blocks, so that the DCT block 25 can perform the field or the frame based DCT depending on the mode. The quantization parameter provided to the Q block 30 is utilized in adjusting the coarseness/fineness of the quantization and thereby controls the fullness of the buffer 60.

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L12: Entry 16 of 78 File: USPT Apr 20, 1999

DOCUMENT-IDENTIFIER: US 5896099 A
TITLE: Audio decoder with buffer fullness control

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L12: Entry 17 of 78 File: USPT Jan 12, 1999

DOCUMENT-IDENTIFIER: US 5859660 A
TITLE: Non-seamless splicing of audio-video transport streams

Detailed Description Text (7):
It should be noted that the behavior of the encoder and decoder buffers is generally tightly coupled. The sum of the encoder buffer fullness plus the decoder buffer fullness a short fixed time later is substantially constant. This means that when the encoder buffer is nearly empty, a short time later the decoder buffer will be nearly full. Conversely, when the encoder buffer is nearly full, a short time later the decoder buffer will be nearly empty. The encoder can therefore control the splice decoding delay .PSI. by controlling the fullness of its own buffer. For example, the encoder can force small splice decoding delays by stuffing the picture preceding the splice point. This will force the decoder buffer fullness to be relatively low at the splice point, resulting in a short splice decoding delay.

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L12: Entry 19 of 78 File: USPT Oct 20, 1998

DOCUMENT-IDENTIFIER: US 5825778 A
**** See image for Certificate of Correction ****
TITLE: VSB modulator input interfrace using simple standard

Detailed Description Text (10):
The filler packet inserter 20, under control of the buffer fullness monitor inserts a filler packet when there is an underflow (shortage of data) condition and generates an SOP signal for the inserted filler packet. Otherwise, it will read in the data from the FIFO.

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L3: Entry 18 of 59 File: USPT Jul 27, 1999

DOCUMENT-IDENTIFIER: US 5929927 A
TITLE: Method and apparatus for providing a modulated scroll rate for text display

Application Filing Date (1):
19961219

Detailed Description Text (19):
In particular, the TOP.sub.-- DISPLAYED.sub.-- ROW signal is coupled to a truncating circuit 433 which outputs only the four MSBs of signal TOP.sub.-- DISPLAYED.sub.-- ROW to produce signal TOP.sub.-- DISPLAYED.sub.-- CHAR.sub.-- ROW. Subtractor 434 subtracts the value of signal TOP.sub.-- DISPLAYED.sub.-- CHAR.sub.-- ROW plus one from the latched (latched by D flip-flop 432) value of the last completed row written to the circular buffer that is provided by the LAST.sub.-- COMPLETED.sub.-- ROW signal. The LAST.sub.-- COMPLETED.sub.-- ROW signal is generated by the buffer write circuitry included in block 302 in FIG. 3. As the signal name indicates, LAST.sub.-- COMPLETED.sub.-- ROW is the row address of the buffer row that was most recently filled with data. Truncation circuit 435 selects the four LSBs of the difference value output by subtractor 434 to produce signal BUFFER.sub.-- FULLNESS which represents the fullness of the buffer. BUFFER.sub.-- FULLNESS is equal to zero when the value of LAST.sub.-- COMPLETED.sub.-- ROW is one more than the value of TOP.sub.-- DISPLAYED.sub.-- CHAR.sub.-- ROW. BUFFER.sub.-- FULLNESS equal to zero indicates that there is no previously undisplayed data in the buffer. Signal BUFFER.sub.-- FULLNESS is coupled to home position pause generator 404 because home position pause duration is determined in response to the BUFFER.sub.-- FULLNESS value.